TEMPLAR®
secure systems

Enterprise 2.5-inch U.3, 3 DWPD, High Performance TCG Opal 2.0 SSD

Technical Specification

Revision History

Revision	Draft Date	History	Author
1.0	2023/06/10	First Release	C. Walker
1.1	2023/08/23	Added 25.6 TB drive data	C. Walker
1.2	2023/09/22	Added additional 25.6 TB drive data	C. Walker

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1. PREFACE

1.1. PRODUCT OVERVIEW

TMP4860 TNC4860

- **Capacities**
  - OP=28%: 800, 1600, 3200, 6400, 12800, 25600 GB
- **Form Factor**
  - U.2/U.3 15mm
- **PCIe Interface**
  - PCIe Gen 4x4
  - Single Port x4 lanes/Dual Port x2 lanes
  - PCIe AER (Advanced Error Reporting)
- **Performance**
  - Maximum Sequential Read/Write
  - Maximum Random Read/Write
  - Latency (Sustained workload)
  - IOPS Consistency
  - QoS (Quality of Service,99% and 99.999%)[1]
- **Power Consumption**[2]
  - Active Power: 25 W
  - Inrush Current: 1.5A
  - Idle Power: 6.0 W / 8.0 W (16T)
- **DWPD: 3**
- **TBW**[3]
  - 800GB SSD – 4380 TB
  - 1600GB SSD – 8760 TB
  - 3200GB SSD – 17520 TB
  - 6400GB SSD –35040 TB
  - 12800GB SSD – 70080 TB
  - 25600GB SSD – 140160 TB
- **MTBF**[4]
- **UBER**
- **Advanced Flash Management**
  - ECC
  - Static and Dynamic Wear Leveling
  - Bad Block Management
  - Deallocate (TRIM) Command
  - S.M.A.R.T.
  - Over-Provision
  - Firmware Update
- **Power Management**
  - Support APST
  - Support ASPM
  - Support L1.2
- **Temperature Range**
  - Operation: 0°C ~ 70°C with specified airflow
  - Storage: -40°C ~ 85°C
- **RoHS compliant**
- **Enterprise Features Support List:**
  - Namespace
  - Dual Port
  - Reservation
  - Metadata Protection Thermal Throttling
  - Power Loss Protection
- **Hardware AES-XTS 256-bit Encryption**
- **Support SMBus**
- **Support NVMe-MI (Management Interface)**
- **Data Retention - 3 months**
- **Physical Dimension:**
  - U.2/U.3 15mm 100(L)x70(W)x15(H) mm^3
  - U.2/U.3 7mm 100(L)x70(W)x7(H) mm^3
- **Compliance**
  - PCIe Express Base 4.0
  - NVMe Express 1.4
  - NVMe Express Management Interface Rev 1.1

[1]Please see Quality of Service (QoS=99%), page 16 and General Description, page 7 for details.

[2]Please see Power Consumption, page 21 for details.

[3]Please see TBW (Terabytes Written) and DWPD (Drive Writes Per Day), page 19 for details.

[4]MTBF is a prediction simulation based on Telcordia SR-332 model.

2. INTRODUCTION

2.1. GENERAL DESCRIPTION

The TEMPLAR U.3 Enterprise SSD Series delivers all the advantages of flash disk technology with PCIe Gen4 x4 interface, including being fully compliant with standard U.2/U.3 form factor, providing low power consumption compared to traditional hard drive and hot-swapping when removing/replacing/upgrading flash disks. The TEMPLAR U.3 Enterprise SSD Series offers a wide range of capacities up to 25,600 GB and its performance can reach up to 7000 MB/s (for sequential read) and 7000 MB/s (for sequential write) based on SK hynix V6 eTLC NAND flash with the DDR4. Moreover, the power consumption of the TEMPLAR U.3 Enterprise SSD Series is much lower than traditional hard drives, making it the best embedded solution for new platforms.

2.2. PRODUCT SERIES NAMING RULES

The following table describes the elements that make up each part number. The lists below the table describe each element.

Table 1. Product Series Naming Schema

DIG	-	Bus Type	Drive Form Factor	Grade	-	Capacity
The first 3 letters of "TEMPLAR"		PG4	U3	Various characteristics		Storage size

Bus Type

- PG4 = PCIe Gen 4

Drive Form Factors

- U3 = U.3

Grade

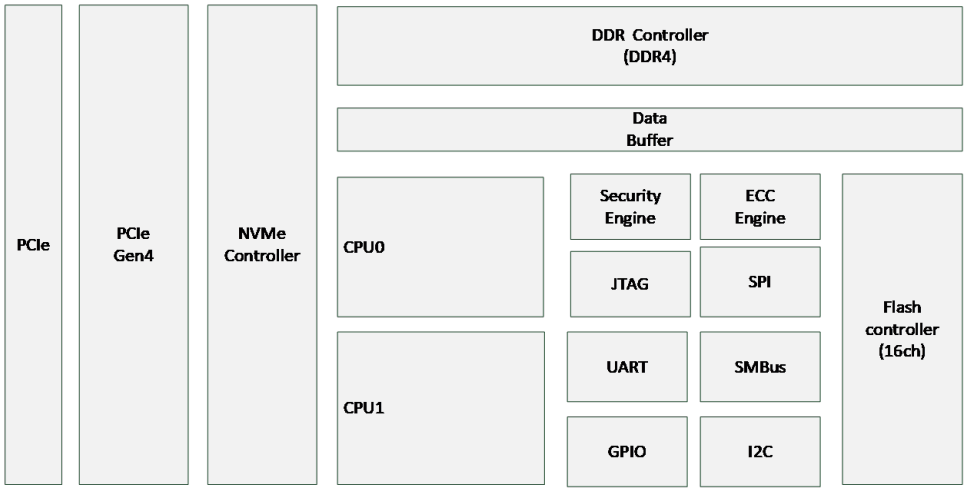
- 25 = Enterprise (NVMe) w/PFail TMP1150/4860, DWPD=3, Opal

Capacity

- 800 = 800GB
- 1600 = 1.6TB
- 3200 = 3.2TB
- 6400 = 6.4TB
- 12800 = 12.8TB
- 25600 = 25.6TB

2.3. CONTROLLER BLOCK DIAGRAM

Figure 1. TEMPLAR U.3 Enterprise SSD Series Controller Block Diagram



2.4. PRODUCT BLOCK DIAGRAM

Figure 2. TEMPLAR U.3 Enterprise SSD Series Product Block Diagram - Front Side

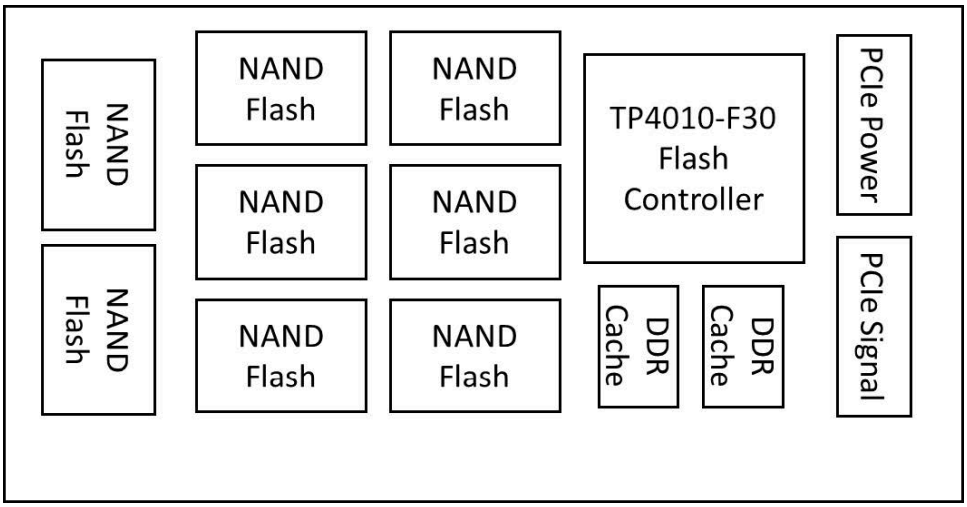
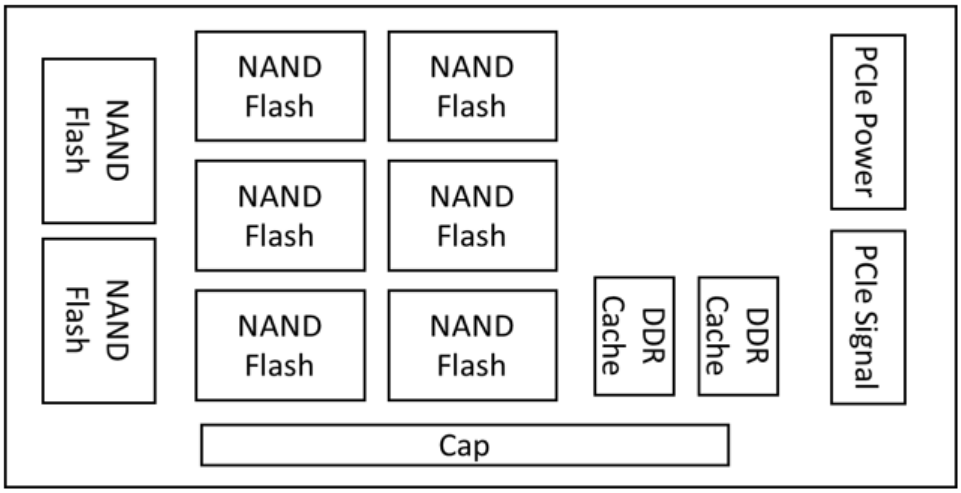


Figure 3. TEMPLAR U.3 Enterprise SSD Series Product Block Diagram - Back Side



2.5. FLASH MANAGEMENT

2.5.1. ERROR CORRECTION CODE (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, the TEMPLAR U.3 Enterprise SSD Series SSD applies the fourth generation LDPC (Low Density Parity Check) of ECC algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

2.5.2. WEAR LEVELING

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

TEMPLAR provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

2.5.3. BAD BLOCK MANAGEMENT

Bad blocks are blocks that do not function properly or contain more invalid bits causing stored data unstable, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Early Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. TEMPLAR implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages bad blocks that appear with use. This practice prevents data being stored into bad blocks and further improves the data reliability.

2.5.4. TRIM

TRIM is a feature that helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space

gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

2.5.5. S.M.A.R.T.

S.M.A.R.T., an acronym for Self-Monitoring, Analysis, and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by S.M.A.R.T., users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, S.M.A.R.T. can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

2.5.6. OVER-PROVISION

Over Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible and cannot be used by users. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

2.5.7. FIRMWARE UPGRADE

Firmware is a set of instructions on how the device communicates with the host. Firmware is upgraded when new features are added, compatibility issues are fixed, or read/write performance gets improved.

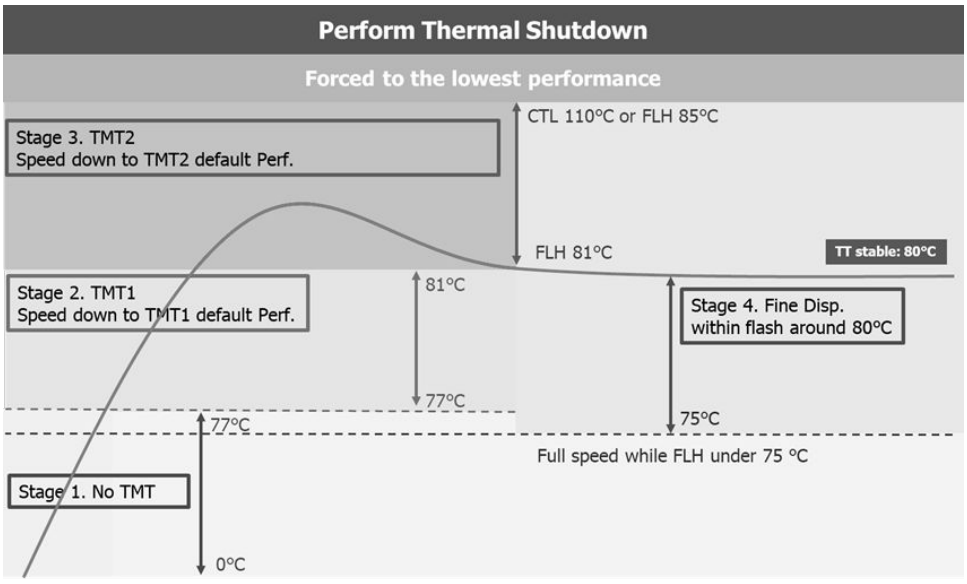
2.5.8. THERMAL THROTTLING

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. The TEMPLAR U.3 Enterprise SSD Series is designed with multiple on-board thermal sensors and with their accuracy, firmware can apply different levels of throttling to achieve the purpose of protection efficiently and proactively via SMART reading.

Table 2. Thermal Throttling Mechanism

Item	Contents
Stage 1 No TMT	To monitor temperature every 1 secs, until flash temperature is over 77 °C. Clock frequency mode 0
Stage 2 TMT1	When flash temp reaches TMT1 (flash 77 °C), the drive will speed down to TMT1 performance(< 2000MB/s).
Stage 3 TMT2	When flash temp reaches TMT2 (flash 81 °C), the drive will speed down to TMT2 performance(< 450MB/s).
Stage 4 TT Stable	Enter TT Dynamic Mechanism (keep TMT1 state 60 sec or TMT2 state 15 sec) Once CTRL (+/- 2) or FLH (+/- 1) temp change: 3% increase or decline of full performance in TMT1 to TMT2 temp range (75~81°C) 3% increase or 9% decline of full performance in TMT2 to Protect temp range (81~85°C)
TMT Protect	When the controller is over 110°C or flash is over 85°C , the drive will be forced to perform at the lowest performance (< 50 MB/s)
TMT Fatal	Perform thermal shutdown process when controller T_J is 120°C.
Resume No TMT	While flash is cooled down to 75°C or below, the performance will be back to full speed.

Figure 4. Thermal Throttling Mechanism



Notes

1. The temperature for TMT is based on T_{case}. (T_{case}: temperate value of on SSD thermal sensor)
2. TMT levels maybe varying by different workloads.

2.6. ADVANCED DEVICE SECURITY FEATURES

2.6.1. SECURE ERASE

Secure Erase is a standard ATA command and will write all “0xFF” to fully wipe all the data on hard drives and SSDs. When this command is issued, SSD controller will erase its storage blocks and return to its factory default settings.

2.6.2. PHYSICAL PRESENCE SID (PSID)

Physical Presence SID (PSID) is defined by TCG as a 32-character string and the purpose is to revert SSD back to its manufacturing setting. PSID code is printed on an SSD label.

2.6.3. CRYPTO ERASE

Crypto Erase (TCG) is a feature that erases all data of an OPAL-activated SSD drive by resetting the cryptographic key of the disk. Since the key is modified, the previously encrypted data will become useless, achieving the purpose of data security.

2.6.4. TCG OPAL

Trusted Computing Group (TCG) provides a scalable infrastructure for managing the encryption of user data in a Storage Device, as well as extensibility to enable the feature. One set of capabilities defined in the Core Spec includes mechanisms for managing access control to user data stored on the Storage Device, including controlling media encryption, Key Management, and Read/Write Lock State.

Table 3. Drive Security Type

Drive Security Type	AES-256 Encryption	Sanitize Operation			TCG Commands	
		Overwrite	Block Erase	Crypto Erase	PSID Revert Process	Instant Security Erase
SED (TCG Opal)	Yes	No	Yes	Yes	Yes[1]	Yes[2]

[1]Crypto Erase is a feature that erases all data of AES encrypted data structure by resetting the cryptographic key of the disk. The previously encrypted data will become irretrievable.

[2]Instant Security Erase is a feature that erases all data of SED drive with Opal-activated encrypted data structure by reverting SSD with PSID. Since the key is reset, the previously encrypted data cannot be accessed anymore.

2.7. SSD LIFETIME MANAGEMENT

2.7.1. TERABYTES WRITTEN (TBW)

TBW (Terabytes Written) is a measurement of an SSD's expected lifespan, which represents the amount of data written to the device. To calculate the TBW of an SSD, the following equation is applied:

TBW = [*DWPD* x *SSD Capacity (GB)* x (*Warranty Days*)] / *1000*

- *DWPD:* Drive writes per day
- *SSD Capacity:* The SSD capacity is the specific capacity in total of an SSD.
- *Warranty Days: Years* x *365 days*

TBW in this document is based on 4K random write.

2.7.2. MEDIA WEAR INDICATOR

Actual life indicator reported by S.M.A.R.T./Health Information Log Page (02h) LIfe Remaining by percentage.

2.7.3. READ ONLY MODE (END OF LIFE)

When a drive is aged by cumulated program/erase cycles, media wear-out may cause increasing numbers of bad blocks over time. When the number of usable good blocks falls outside a defined usable range, the drive will notify the Host through AER event and Critical Warning to enter Read Only Mode to prevent further data corruption. The user should immediately replace the drive.

3. PRODUCT SPECIFICATIONS

3.1. ELECTRICAL/PHYSICAL INTERFACE

- PCIe Interface
- Compliant with NVMe 1.4
- PCIe Express Base Ver 4.0
- PCIe Gen 4 x 4 lanes & backward compatible to PCIe Gen 3, Gen 2 and Gen 1 Device Capacity

Table 4. User Capacity and Addressable Sectors

Capacity	User Addressable Sectors	Bytes per Sector
800 GB	1,562,824,368	512 Bytes
1.6 TB	3,125,627,568	
3.2 TB	6,251,233,968	
6.4 TB	12,502,446,768	
12.8 TB	25,004,872,368	
25.6 TB	50,009,723,568	

Notes

1. 1 Gigabyte (GB) is equal to 1,000,000,000 bytes; 1 sector is equal to 512 bytes.
2. The total actual usable capacity of the SSD may be less than the total physical capacity because internal NAND management, SSD format, SSD partition, operating system and so on.
3. The count of User Addressable Sectors is calculated by the formula of IDEMA.

3.2. PERFORMANCE

Table 5. 15mm High Performance Sequential Read/Write Performance and 4K Sustained Random Read/ Write Performance

Capacity	Maximum Performance			
	Sequential 128KB (QD=32, Workers=1)		4K Sustained Random (QD=64, Workers=8)	
800 GB	7,000	1,700	1,000,000	120,000
1.6 TB	7,000	3,400	1,600,000	270,000
3.2 TB	7,000	6,700	1,600,000	420,000
6.4 TB	7,000	6,700	1,600,000	440,000
12.8 TB	7,000	6,700	1,600,000	470,000
25.6 TB	7,000	6,000	1,600,000	170,000

Notes

1. Performance may differ according to flash configuration and platform.
2. The tables are for reference only. Any criteria for accepting goods shall be further discussed based on different flash configurations.

3.3. LATENCY

Table 6. High Performance 4KB Sustained Random Read/Write Latency

Capacity	4K Sustained Random (QD=1, Workers=1)		4K Sustained Random (QD=32, Workers=1)		4K Sustained Random (QD=64, Workers=8)	
	Read	Write	Read	Write	Read	Write
	µs	*µs*	*µs*	*µs*	*µs*	*µs*
800 GB	95	15	100	270	550	4350
1.6 TB	95	15	100	140	310	2000
3.2 TB	95	15	100	80	310	1250
6.4 TB	95	15	100	80	310	1250
12.8 TB	95	15	100	80	310	1100
25.6 TB	95	15	100	90	310	1250

Notes

1. Performance was estimated based on SK hynix V6 eTLC NAND flash.
2. Performance may differ according to flash configuration and platform.
3. The tables are for reference only. Any criteria for accepting goods shall be further discussed based on different flash configurations.

3.4. IOPS CONSISTENCY

Table 7. 15mm High Performance 4KB Sustained Random Read/Write IOPS Consistency

Capacity	4K Sustained Random (QD=1, Workers=1)		4K Sustained Random (QD=32, Workers=1)		4K Sustained Random (QD=64, Workers=8)	
	Read	Write	Read	Write	Read	Write
	%	%	%	%	%	%
800 GB	95	95	95	95	95	95
1.6 TB	95	95	95	95	95	95
3.2 TB	95	95	95	95	95	95
6.4 TB	95	95	95	95	95	95
12.8 TB	95	95	95	95	95	95
25.6 TB	95	95	95	95	95	95

Notes

1. Consistency Definition: 100 - [(mean_IOPS - min_IOPS) / mean_IOPS]
2. Performance was estimated based on SK hynix V6 eTLC NAND flash.
3. Performance may differ according to flash configuration and platform.
4. The tables are for reference only. Any criteria for accepting goods shall be further discussed based on different flash configurations

3.5. QUALITY OF SERVICE (QOS=99%)

Table 8. 15mm High Performance: 4KB Sustained Random Read/Write Quality of Service (QoS=99%) 1ms =1000us

Capacity	4KB Sustained Random Read/Write Quality of Service (QoS=99%)					
	(QD=1, Workers=1)		(QD=32, Workers=1)		(QD=64, Workers=8)	
	Read (4KB)	Write (4KB)	Read (4KB)	Write (4KB)	Read (4KB)	Write (4KB)
	µs	*µs*	*µs*	*µs*	*µs*	*µs*
800 GB	100	13	200	270	2400	4500
1.6 TB	100	13	160	120	1000	2000
3.2 TB	100	13	140	100	600	2000
6.4 TB	100	13	130	100	600	1800
12.8 TB	100	13	120	90	600	1600
25.6 TB	100	13	120	110	600	1600

3.6. WEIGHT

Table 9. 15mm Weight

Capacity	Flash Configuration	Flash Type	Weight (g)
800 GB	256 GB x 4	16CE, 512Gb, QDP	195
1.6 TB	256 GB x 16	32CE, 512Gb, QDP	196
3.2 TB	256 GB x 16	64CE, 512Gb QDP	198
6.4 TB	512 GB x 16	128CE, 512Gb ODP	200
12.8 TB	512 GB x 32	128CE, 512Gb ODP	203
25.6 TB	1024 GB x 32	128CE, 512Gb HDP	205

4. ENVIRONMENTAL SPECIFICATIONS

4.1. TEMPERATURE AND HUMIDITY

Table 10. Temperature and Humidity Specification

	Temperature	Relative Humidity
Operating	0°C to 70°C	5% to 95%
Non-operating	-40°C to 85°C	5% to 95%

4.2. SHOCK

Table 11. Shock

	Acceleration	Pulse Duration
Operating	500G	2ms
	1000G	1000ms
Non-operating	500G	2ms
	1000G	1000ms

4.3. VIBRATION

Table 12. Vibration

	Frequency	Amplitude
Operating	200 to 2000 H	2.17 Grms
Non-operating	10 - 2000 Hz	16.3 Grms
	2 -5 - 500 Hz	3 Grms

4.4. ALTITUDE

Table 13. Altutude

	Value
Operating	0 to 18,000 feet
Non-operating	0 to 40,000 feet

4.5. TBW (TERABYTES WRITTEN) AND DWPD (DRIVE WRITES PER DAY)

Table 14. TBW & DWPD

Capacity	Flash Structure	Flash Type	TBW	DWPD
800 GB	256GB x 4	3D eTLC	4380	3
1.6 TB	256GB x 8	3D eTLC	8760	3
3.2 TB	256GB x 16	3D eTLC	17520	3
6.4 TB	512GB x 16	3D eTLC	35040	3
12.8 TB	512GB x 32	3D eTLC	70080	3
25.6 TB	512GB x 32	3D eTLC	140160	3

4.6. POWER ON/OFF CYCLES

The definition of power on/off cycles is that the power is withdrawn from the SSD device and then restored. The test is to simulate the behavior that the SSD still can be restored and active normally when host platforms go into suspend and shutdown.

During the Power On/Off cycles test, the SSD can be protective if the SSD encounters 24 times of power on/off per day within warranty period.

4.7. UBER

Table 15. UBER

Capacity	Flash Type	UBER
800 GB	3D NAND	< 1 sector per 10^{18} bits read
1.6 TB		
3.2 TB		
6.4 TB		
12.8 TB		
25.6 TB		

Notes

1. UBER (Uncorrectable Bit Error Rates) means the uncorrectable error per bits read.

4.8. MEAN TIME BETWEEN FAILURES

Mean Time Between Failures (MTBF) is demonstrated through a 2,000-hour Reliability Demonstration Test.

Table 16. MTBF

Specification	Value
Mean Time Between Failures	2.4 million hours

5. ELECTRICAL SPECIFICATIONS

5.1. SUPPLY VOLTAGE

Table 17. Supply Voltage

	All Capacities
12v	+/- 10%
12v noise level	240mVp-p, 0-20MHz
12v min off time	500ms
3.3v aux	+/- 15%

Notes

1. Minimum time between power removed from SSD (Vcc < 100 mV) and power re-applied to the drive.

5.2. POWER CONSUMPTION

Table 18. Power Consumption

Capacity	Random Read (Typ.,W)	Random Write (Typ.,W)	Sequential Read(Typ.,W)	Sequential Write(Typ., W)	Idle (Typ., W)
800 GB	8.9	8.6	9.3	8.4	4.90
1.6 TB	12.9	12.4	10.5	13.4	5.52
3.2 TB	13.9	16.5	11.1	18.4	5.83
6.4 TB	16.0	17.7	11.8	19.8	5.87
12.8 TB	16.6	20.1	12.7	20.9	7.43
25.6 TB	18.6	20.3	13.7	20.2	8.45

Notes

1. Power consumption is measured on full speed mode.

5.3. INRUSH CURRENT

Table 19. Inrush Current

Inrush current	800GB	1.6 TB	3.2 TB	6.4 TB	12.8 TB	25.6 TB
12v	1.5A					

6. INTERFACE

6.1. PIN ASSIGNMENT AND DESCRIPTIONS

Figure 5. U.3 PCIe SSD Pin Assignment

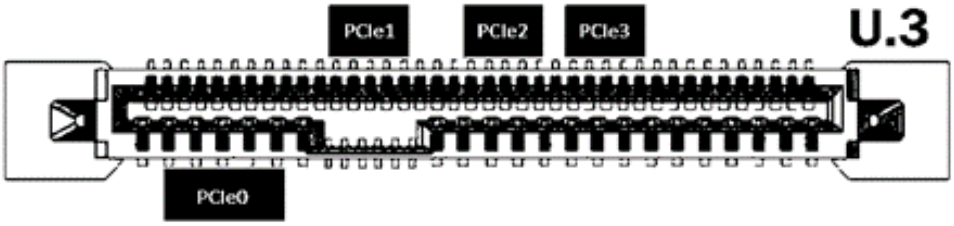


Figure 6. U.2 PCIe SSD Pin Assignment

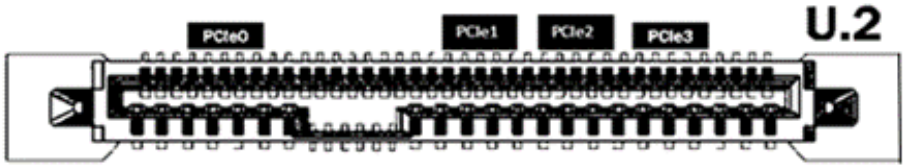


Table 20. Pin Assignment and Description of the TEMPLAR U.3 Enterprise SSD Series

Pin No.	Name	Type	Description
P1	WAKE#	Input	Reserved
P2	Reserved	Reserved	Reserved
P3	PWRDIS	Output	Power disable
P4	IfDet#	Input	Input type detect
P5	Ground	Ground	Ground
P6	Ground	Ground	Ground
P7	+5V	Power	Reserved
P8	+5V	Power	Reserved
P9	+5V	Power	Reserved
P10	PRSNT#	Input	Presence detect
P11	Activity#	Input	Activity indicator
P12	Ground	Ground	Ground
P13	+12V Precharge	Power	+12V precharge power
P14	+12V	Power	+12V power
P15	+12V	Power	+12V power
SG1	Ground	Ground	Ground
SG2	Ground	Ground	Ground
S1	Ground	Ground	Ground
S2	U.3 TX p0	Diff-Pair	Transmitter differential pair, U.3 lane 0
S3	U.3 TX n0	Diff-Pair	Transmitter differential pair, U.3 lane 0
S4	Ground	Ground	Ground
S5	U.3 RX n0	Diff-Pair	Receiver differential pair, U.3 lane 0
S6	U.3 RX p0	Diff-Pair	Receiver differential pair, U.3 lane 0
S7	Ground	Ground	Ground
S8	Ground	Ground	Ground
S9	U.3 TX p1	Diff-Pair	Transmitter differential pair, U.3 lane 1
S10	U.3 TX n1	Diff-Pair	Transmitter differential pair, U.3 lane 1
S11	Ground	Ground	Ground
S12	U.3 RX n1	Diff-Pair	Receiver differential pair, U.3 lane 1
S13	U.3 RX p1	Diff-Pair	Receiver differential pair, U.3 lane 1
S14	Ground	Ground	Ground
S15	HPT0	Output	Host port type
S16	Ground	Ground	Ground
S17	U.3 TX p2/U.2 TX p1	Diff-Pair	Transmitter differential pair, U.3 lane 2, or U.2 lane 1

Pin No.	Name	Type	Description
S18	U.2 TX n2/U.2 TX n1	Diff-Pair	Transmitter differential pair, U.3 Lane 2, or U.2 lane 1
S19	Ground	Ground	Ground
S20	U.3 RX n2/U.2 RX n1	Diff-Pair	Receiver differential pair, U.3 lane 2, or U.2 lane 1
S21	U.3 RX p2/U.2 RX p1	Diff-Pair	Receiver differential pair, U.3 lane 2, or U.2 lane 1
S22	Ground	Ground	Ground
S23	U.3 TX p3/U.2 TX p2	Diff-Pair	Transmitter differential pair, U.3 lane 3, or U.2 lane 2
S24	U.3 TX n3/U.2 TX n2	Diff-Pair	Transmitter differential pair, U.3 lane 3, or U.2 lane 2
S25	Ground	Ground	Ground
S26	U.3 RX n3/U.2 RX n2	Diff-Pair	Receiver differential pair, U.3 lane 3, or U.2 lane 2
S27	U.3 RX p3/U.2 RX p2	Diff-Pair	Receiver differential pair, U.3 lane 3, or U.2 lane 2
S28	Ground	Ground	Ground
E1	REFCLKB+	Diff-Pair	Reference clock (differential pair) for second X2 port
E2	REFCLKB-	Diff-Pair	Reference clock (differential pair) for second X2 port
E3	+3.3 Vaux	Power	3.3 V auxiliary power
E4	CLKREQ#/PERSTB#	Bi-dir	Clock request/Fundamental reset for second x2 port
E5	PERST#	Output	Fundamental reset (if dual port mode enabled, first x2 port)
E6	IFDet2#	Input	Interface type detect
E7	REFCLK+	Diff-Pair	Reference clock (if dual-port enabled, first X2 port)
E8	REFCLK-	Diff-Pair	Reference clock (if dual-port enabled, first X2 port)
E9	Ground	Ground	Ground
E10	U.2 TX p0	Diff-Pair	Transmitter differential pair, U.2 lane 0
E11	U.2 TX n0	Diff-Pair	Transmitter differential pair, U.2 lane 0
E12	Ground	Ground	Ground
E13	U.2 RX n0	Diff-Pair	Receiver differential pair, U.2 lane 0
E14	U.2 RX p0	Diff-Pair	Receiver differential pair, U.2 lane 0
E15	Ground	Ground	Ground
E16	HPT1	Output	Hot port type

Pin No.	Name	Type	Description
E17	U.2 TX p3	Diff-Pair	Transmitter differential pair, U.2 lane 3
E18	U.2 TX n3	Diff-Pair	Transmitter differential pair, U.2 lane 3
E19	Ground	Ground	Ground
E20	U.2 RX n3	Diff-Pair	Receiver differential pair. U.2 lane 3
E21	U.2 RX p3	Diff-Pair	Receiver differential pair, U.2 lane 3
E22	Ground	Ground	Ground
E23	SMCLK	Bi-Dir	SMBus (system management bus) clock
E24	SMDAT	Bi-Dir	SMBus (system management bus) data
E25	DualPortEn#	Output	Dual-port mode

7. SUPPORTED COMMANDS

7.1. NVME COMMAND LIST

Table 21. Admin Command List

Identifier	O/M	Supported	Command Description
00h	M	Y	Delete I/O Submission Queue
01h	M	Y	Create I/O Submission Queue
02h	M	Y	Get Log Page
04h	M	Y	Delete I/O Completion Queue
05h	M	Y	Create I/O Completion Queue
06h	M	Y	Identify
08h	M	Y	Abort
09h	M	Y	Set Feature
0Ah	M	Y	Get Feature
0Ch	M	Y	Asynchronous Event Request
0Dh	O	Y	Namespace Management
10h	O	Y	Firmware Commit
11h	O	Y	Firmware Image Download
14h	O	Y	Device Self-test
15h	O	Y	Namespace Attachment
18h	O	N	Keep Alive
19h	O	-	Directive Send
1Ah	O	-	Directive Receive
1Ch	O	-	Virtualization Management
1Dh	O	Y	NVMe-MI Send
1Eh	O	Y	NVMe-MI Receive
7Ch	O	-	Doorbell Buffer Config
80h	O	Y	Format NVM
81h	O	Y	Security Send
82h	O	Y	Security Receive
84h	O	Y	Sanitize
86h	O	-	Get LBA Status

Table 22. I/O Commands

Identifier	O/M	Supported	Command Description
00h	O	Y	Flush
01h	O	Y	Write
02h	O	Y	Read
04h	O	Y	Write Uncorrectable
05h	O	Y	Compare
08h	O	Y	Write Zeroes
09h	O	Y	Dataset Management (Trim Only)
0Ch	O	Y	Verify
0Dh	O	Y	Reservation Register
0Eh	O	Y	Reservation Report
11h	O	Y	Reservation Acquire
15h	O	Y	Reservation Release

Table 23. Set Feature Commands

Identifier	O/M	Supported	Command Description
00h	-	-	Reserved
01h	M	Y	Arbitration
02h	M	Y	Power Management
03h	O	-	LBA Range Type
04h	M	Y	Temperature Threshold
05h	M	Y	Error Recovery
06h	O	Y	Volatile Write Cache
07h	M	Y	Number Of Queues
08h	M	Y	Interrupt Coalescing
09h	M	Y	Interrupt Vector Configuration
0Ah	M	Y	Write Atomicity Normal
0Bh	M	Y	Asynchronous Event Configuration
0Ch	O	-	Autonomous Power State Transition
0Dh	O	-	Host Memory Buffer
0Eh	O	Y	Timestamp
0FH	O	Y	Keep Alive Timer
10h	O	-	Host Controlled Thermal Management
11h	O	-	Non-Operational Power State Config
12h	O	-	Read Recovery Level Config
13h	O	-	Predictable Latency Mode Config
14h	O	-	Predictable Latency Mode Window
15h	O	-	LBA Status Information Attributes
16h	O	-	Host Behavior Support
17h	O	Y	Sanitize Config
18h	O	-	Endurance Group Event Configuration
19h - 77h	-	-	Reserved (NVMe Reserved)
78h - 7Dh	-	-	Reserved (NVMe MI Reserved)
7Eh	M	Y	Controller Metadata (NVMe MI)
7Fh	M	Y	Namespace Metadata (NVMe MI)
80h	O	-	Software Progress Marker
81h	O	Y	Host Identifier
82h	O	Y	Reservation Host Mask
83h	O	Y	Reservation Persistence
84h	O	-	Namespace Write Protection Config
85h - BFh	-	-	Command Set Specific (Reserved)
C0h - FFh	O	-	Vendor Specific

Table 24. Log Page Commands

Identifier	O/M	Supported	Command Description
00h	-	-	Reserved
01h	M	Y	Error Information
02h	M	Y	S.M.A.R.T. / Health Information
03h	M	Y	Firmware Slot Information
04h	O	Y	Changed Namespace List
06h	O	Y	Device Self-test
07h	O	Y	Telemetry Host-Initiated
08h	O	Y	Telemetry Controller-Initiated
09h	O	-	Endurance Group Information
0Ah	O	-	Predictable Latency Per NVM Set
0Bh	O	-	Predictable Latency Event Aggregate
0Ch	O	-	Asymmetric Namespace Access
0Dh	O	Y	Persistent Event Log
0Eh	O	-	LBA Status Information
0Fh	O	-	Endurance Group Event Aggregate
10h - 7Fh	-	-	Reserved
80h	O	Y	Reservation Notification
81h	O	Y	Sanitize Status
82h - FFh	-	-	Reserved

Table 25. NVMe Management Interface Commands

Identifier	O/M	Supported	Command Description
00h	M	Y	Read NVMe-MI Data Structure
01h	M	Y	NVM Subsystem Health Status Poll
02h	M	Y	Controller Health Status Poll
03h	M	Y	Configuration Set
04h	M	Y	Configuration Get
05h	M	Y	VPD Read
06h	M	Y	VPD Write
07h	M	Y	Reset
08h	-	-	SES Receive
09h	-	-	SES Send
0Ah	O	-	Management Endpoint Buffer Read
0Bh	O	-	Management Endpoint Buffer Write
0Ch - BFh	O	-	Reserved
C0h - FFh	O	-	Vendor Specific

NOTES:

1. "Y" means "Supported".
2. "O" means "Option, default Not Supported".
3. "-" means "Not supported".

Table 26. SMBus / I2C Elements Supported

SMBus/I2C Element	SMBus/I2C Address (8bit)	
	Hex Format	Binary Format
FRU Information Device (for NVMe Storage Device)	A6h	1010_011xb
SMBus/I2C Management Endpoint	3Ah	0011_101xb
Basic Management Command	D4h	1101_010xb

7.2. IDENTIFY DEVICE DATA

The following table details the sector data returned by the IDENTIFY DEVICE command.

Table 27. Identify Controller Data Structure

Bytes	O/M	Description	Default Value
01:00	M	PCI Vendor ID (VID)	0x1987
03:02	M	PCI Subsystem Vendor ID (SSVID)	0x1987
23:04	M	Serial Number (SN)	TBD
63:24	M	Model Number (MN)	TBD
71:64	M	Firmware Revision (FR)	TBD
72	M	Recommended Arbitration Burst (RAB)	0x01
75:73	M	IEEE OUI Identifier (IEEE)	TBD[1]
76	O	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)	0x03
77	M	Maximum Data Transfer Size (MDTS)	0x09
79:78	M	Controller ID (CNTLID)	0x0001
83:80	M	Version (VER)	0x00010400
87:84	M	RTD3 Resume Latency (RTD3R)	0x001E8480 (2 sec)
91:88	M	RTD3 Entry Latency (RTD3E)	0x00989680
95:92	M	Optional Asynchronous Events Supported (OAES)	0x00000300
99:96	M	Controller Attributes (CTRATT)	0x00000000
100:100	O	Read Recovery Levels Supported (RRLS)	0x0000
110:102	-	Reserved	0x00
111	M	Controller Type (CNTRLTYPE)	0x01
127:112	O	FRU Globally Unique Identifier (FGUID[16])	TBD
129:128	O	Command Retry Delay Time 1 (CRDT1)	0x0000
131:130	O	Command Retry Delay Time 2 (CRDT2)	0x0000
133:132	O	Command Retry Delay Time 3 (CRDT3)	0x0000
239:134	-	Reserved	-
255:240	-	Refer to the NVMe Management Interface Specification for definition	0x00
257:256	M	Optional Admin Command Support (OACS)	0x005F
258	M	Abort Command Limit (ACL)	0x07
259	M	Asynchronous Event Request Limit (AERL)	0x0E
260	M	Firmware Updates (FRMW)	0x1C
261	M	Log Page Attributes (LPA)	0x1E
262	M	Error Log Page Entries (ELPE)	0x3E
263	M	Number of Power States Support (NPSS)	3

Bytes	O/M	Description	Default Value
264	M	Admin Vendor Specific Command Configuration (AVSCC)	0x01
265	O	Autonomous Power State Transition Attributes (APSTA)	0x00
267:266	M	Warning Composite Temperature Threshold (WCTEMP)	0x0157 (70C)
269:268	M	Critical Composite Temperature Threshold (CCTEMP)	0x0161 (80C)
271:270	O	Maximum Time for Firmware Activation (MTFA)	0x0032
275:272	O	Host Memory Buffer Preferred Size (HMPRE)	0x00000000
279:276	O	Host Memory Buffer Minimum Size (HMMIN)	0x00000000
295:280	O	Total NVM Capacity (TNVMCAP)	See footnote[2]
311:296	O	Unallocated NVM Capacity (UNVMCAP)	See footnote[2]
315:312	O	Replay Protected Memory Block Support (RPMBS)	0x00000000
317:316	O	Extended Device Self-test Time (EDSTT)	0x0002
318	O	Device Self-test Options (DSTO)	0x01
319	O	Firmware Update Granularity (FWUG)	0x01
321:320	O	Keep Alive Support (KAS)	0x0000
323:322	O	Host Controlled Thermal Management Attributes (HCTMA)	0x0001
325:324	O	Minimum Thermal Management Temperature (MNTMT)	0x0111
327:326	O	Maximum Thermal Management Temperature (MXTMT)	0x0157
331:328	O	Sanitize Capabilities (SANICAP)	0x60000003
335:332	O	Host Memory Buffer Min. Descriptor Entry Size (HMMINDS)	0x00000000
337:336	O	Host Memory Maximum Descriptors Entries (HMMAXD)	0x0000
339:338	O	NVM Set ID Maximum (NSETIDMAX)	0x0000
341:340	O	Endurance Group ID Maximum (ENDGIDMAX)	0x0000
342	O	ANA Maximum Transition Time (ANATT)	0x00
343	O	Asymmetric Namespace Access Capabilities (ANACAP)	0x00
347:344	O	ANA Group Identifier Maximum (ANAGRPMAX)	0x0000

Bytes	O/M	Description	Default Value
351:348	O	Number of ANA Group Identifiers (NANAGRPID)	0x00000000
355:352	O	Persistent Event Log Size (PELS)	0x63
511:356	-	Reserved	0x0

[1]The OUI shall be a valid IEEE/RAC assigned identifier that may be registered at http://standards.ieee.org/develop/regauth/oui/public.html

[2]Depends on the using of capacity

Table 28. NVM Command Set Attributes

Bytes	O/M	Description	Default Value
512	M	Submission Queue Entry Size (SQES)	0x66
513	M	Completion Queue Entry Size (CQES)	0x44
515:514	-	Maximum Outstanding Commands (MAXCMD)	0x0400 1 port 0x0200 2 port
519:516	M	Number of Namespaces (NN)	0x00000080
521:520	M	Optional NVM Command Support (ONCS)	0x00FF
523:522	M	Fused Operation Support (FUSES)	0x0000
524	M	Format NVM Attributes (FNA)	0x04
525	M	Volatile Write Cache (VWC)	0x07
527:526	M	Atomic Write Unit Normal (AWUN)	0x00FF
529:528	M	Atomic Write Unit Power Fail (AWUPF)	0x00FF
530	M	NVM Vendor Specific Command Configuration (NVSCC)	0x01
531	M	Namespace Write Protection Capabilities (NWPC)	0x00
533:532	O	Atomic Compare & Write Unit (ACWU)	0x0000
535:534	M	Reserved	0x0000
539:536	O	SGL Support (SGLS)	0x000F0001
543:540	O	Maximum Number of Allowed Namespaces (MNAN)	0x00000000
767:544	M	Reserved	0x00
1023:768	M	NVM Subsystem NVMe Qualified Name (SUBNQN)	TBD

Table 29. IO Command Set Attributes

Bytes	O/M	Description	Default Value
2079:2048	M	Power State 0 Descriptor (PSD0)	-
Bit[255:184]	-	Reserved	0x00
Bit[183:182]	-	Active Power Scale (APS)	0x0
Bit[181:179]	-	Reserved	0x0
Bit[178:176]	-	Active Power Workload (APW)	0x0
Bit[175:160]	-	Active Power	0x0
Bit[159:152]	-	Reserved	0x0
Bit[151:150]	-	Idle Power Scale (IPS)	0x0
Bit[149:144]	-	Reserved	0x0
Bit[143:128]	-	Idle Power (IDLP)	0x0
Bit[127:125]	-	Reserved	0x0
Bit[124:120]	-	Relative Write Latency (RWL)	0x0
Bit[119:117]	-	Reserved	0x0
Bit[116:112]	-	Relative Write Throughput (RWT)	0x0
Bit[111:109]	-	Reserved	0x0
Bit[108:104]	-	Relative Read Latency (RRL)	0x0
Bit[103:101]	-	Reserved	0x0
Bit[100:96]	-	Relative Read Throughput (RRT)	0x0
Bit[95:64]	-	Exit Latency (EXLAT)	0x0
Bit[63:32]	-	Entry Latency (ENLAT)	0x0
Bit[31:26]	-	Reserved	0x0
Bit[25]	-	Non-Operational State (NOPS)	0
Bit[24]	-	Max Power Scale (MPS)	0
Bit[23:16]	-	Reserved	0x0
Bit[15:0]	-	Maximum Power (MP)	0x37A
2111:2080	O	Power State 1 Descriptor (PSD1)	-
Bit[255:184]	-	Reserved	0x00
Bit[183:182]	-	Active Power Scale (APS)	0x0
Bit[181:179]	-	Reserved	0x0
Bit[178:176]	-	Active Power Workload (APW)	0x0
Bit[175:160]	-	Active Power (ACTP)	0x0
Bit[159:152]	-	Reserved	0x0
Bit[151:150]	-	Idle Power Scale (IPS)	0x0
Bit[149:144]	-	Reserved	0x0
Bit[143:128]	-	Idle Power (IDLP)	0x0
Bit[127:125]	-	Reserved	0x0

Bytes	O/M	Description	Default Value
Bit[124:120]	-	Relative Write Legacy (RWL)	0x1
Bit[119:117]	-	Reserved	0x0
Bit[116:112]	-	Relative Write Throughput (RWT)	0x1
Bit[111:109]	-	Reserved	0x0
Bit[108:104]	-	Relative Read Latency (RRL)	0x1
Bit[103:101]	-	Reserved	0x0
Bit[100:96]	-	Relative Read Throughput (RRT)	0x1
Bit[95:64]	-	Exit Latency (EXLAT)	0x0
Bit[63:32]	-	Entry Latency (ENLAT)	0x0
Bit[31:26]	-	Reserved	0x0
Bit[25]	-	Non-Operational State (NOPS)	0
Bit[24]	-	Max Power Scale (MPS)	0
Bit[23:16]	-	Reserved	0x0
Bit[15:0]	-	Maximum Power (MP)	0xE6
2143:2112	O	Power State 2 Descriptor (PSD2)	-
Bit[255:184]	-	Reserved	0x00
Bit[183:182]	-	Active Power Scale (APS)	0x0
Bit[181:179]	-	Reserved	0x0
Bit[178:176]	-	Active Power Workload (APW)	0x0
Bit[175:160]	-	Active Power (ACTP)	0x0
Bit[159:152]	-	Reserved	0x0
Bit[151:150]	-	Idle Power Scale (IPS)	0x0
Bit[149:144]	-	Reserved	0x0
Bit[143:128]	-	Idle Power (IDLP)	0x0
Bit[127:125]	-	Reserved	0x0
Bit[124:120]	-	Relative Write Latency (RWL)	0x2
Bit[119:117]	-	Reserved	0x0
Bit[116:112]	-	Relative Write Throughput (RWT)	0x2
Bit[111:109]	-	Reserved	0x0
Bit[108:104]	-	Relative Read Latency (RRL)	0x2
Bit[103:101]	-	Reserved	0x0
Bit[100:96]	-	Relative Read Throughput (RRT)	0x2
Bit[95:64]	-	Exit Latency (EXLAT)	0x0
Bit[63:32]	-	Entry Latency (ENLAT)	0x0
Bit[31:26]	-	Reserved	0x0
Bit[25]	-	Non-Operational State (NOPS)	0
Bit[24]	-	Max Power Scale (MPS)	0
Bit[23:16]	-	Reserved	0x0

Bytes	O/M	Description	Default Value
Bit[15:0]	-	Maximum Power (MP)	0xB4
2175:2144	O	Power State 3 Descriptor (PSD3)	0x00
Bit[255:184]	-	Reserved	0x00
Bit[183:182]	-	Active Power Scale (APS)	0x0
Bit[181:179]	-	Reserved	0x0
Bit[178:176]	-	Active Power Workload (APW)	0x0
Bit[175:160]	-	Active Power (ACTP)	0x0
Bit[159:152]	-	Reserved	0x0
Bit[151:150]	-	Idle Power Scale (IPS)	0x0
Bit[149:144]	-	Reserved	0x0
Bit[143:128]	-	Idle Power (IDLP)	0x0
Bit[127:125]	-	Reserved	0x0
Bit[124:120]	-	Relative Write Latency (RWL)	0x3
Bit[119:117]	-	Reserved	0x0
Bit[116:112]	-	Relative Write Throughput (RWT)	0x3
Bit[111:109]	-	Reserved	0x0
Bit[108:104]	-	Relative Read Latency (RRL)	0x2
Bit[103:101]	-	Reserved	0x0
Bit[100:96]	-	Relative Read Throughput (RRT)	0x2
Bit[95:64]	-	Exit Latency (EXLAT)	0x0
Bit[63:32]	-	Entry Latency (ENLAT)	0x0
Bit[31:26]	-	Reserved	0x0
Bit[25]	-	Non-Operational State (NOPS)	0
Bit[24]	-	Max Power Scale (MPS)	0
Bit[23:16]	-	Reserved	0x0
Bit[15:0]	-	Maximum Power (MP)	0xB4
2207:2176	O	Power State 4 Descriptor (PSD4)	0x00
Bit[255:184]	-	Reserved	0x00
Bit[183:182]	-	Active Power Scale (APS)	0x0
Bit[181:179]	-	Reserved	0x0
Bit[178:176]	-	Active Power Workload (APW)	0x0
Bit[175:160]	-	Active Power (ACTP)	0x0
Bit[159:152]	-	Reserved	0x0
Bit[151:150]	-	Idle Power Scale (IPS)	0x0
Bit[149:144]	-	Reserved	0x0
Bit[143:128]	-	Idle Power (IDLP)	0x0
Bit[127:125]	-	Reserved	0x0
Bit[124:120]	-	Relative Write Latency (RWL)	0x4

Bytes	O/M	Description	Default Value
Bit[119:117]	-	Reserved	0x0
Bit[116:112]	-	Relative Write Throughput (RWT)	0x4
Bit[111:109]	-	Reserved	0x0
Bit[108:104]	-	Relative Read Latency (RRL)	0x2
Bit[103:101]	-	Reserved	0x0
Bit[100:96]	-	Relative Read Throughput (RRT)	0x2
Bit[95:64]	-	Exit Latency (EXLAT)	0x0
Bit[63:32]	-	Entry Latency (ENLAT)	0x0
Bit[31:26]	-	Reserved	0x0
Bit[25]	-	Non-Operational State (NOPS)	0
Bit[24]	-	Max Power Scale (MPS)	0
Bit[23:16]	-	Reserved	0x0
Bit[15:0]	-	Maximum Power (MP)	0xB4
2239:2208	O	Power State 5 Descriptor (PSD5)	0x00
2271:2240	O	Power State 6 Descriptor (PSD6)	0x00
2303:2272	O	Power State 7 Descriptor (PSD7)	0x00
2335:2304	O	Power State 8 Descriptor (PSD8)	0x00
2367:2336	O	Power State 9 Descriptor (PSD9)	0x00
2399:2368	O	Power State 10 Descriptor (PSD10)	0x00
2431:2400	O	Power State 11 Descriptor (PSD11)	0x00
2463:2432	O	Power State 12 Descriptor (PSD12)	0x00
2495:2464	O	Power State 13 Descriptor (PSD13)	0x00
2527:2496	O	Power State 14 Descriptor (PSD14)	0x00
2559:2528	O	Power State 15 Descriptor (PSD15)	0x00
2591:2560	O	Power State 16 Descriptor (PSD16)	0x00
2623:2592	O	Power State 17 Descriptor (PSD17)	0x00
2655:2624	O	Power State 18 Descriptor (PSD18)	0x00
2687:2656	O	Power State 19 Descriptor (PSD19)	0x00
2719:2688	O	Power State 20 Descriptor (PSD20)	0x00
2751:2720	O	Power State 21 Descriptor (PSD21)	0x00
2783:2752	O	Power State 22 Descriptor (PSD22)	0x00
2815:2784	O	Power State 23 Descriptor (PSD23)	0x00
2847:2816	O	Power State 24 Descriptor (PSD24)	0x00
2879:2848	O	Power State 25 Descriptor (PSD25)	0x00
2911:2880	O	Power State 26 Descriptor (PSD26)	0x00
2943:2912	O	Power State 27 Descriptor (PSD27)	0x00
2975:2944	O	Power State 28 Descriptor (PSD28)	0x00
3007:2976	O	Power State 29 Descriptor (PSD29)	0x00

Bytes	O/M	Description	Default Value
3039:3008	O	Power State 30 Descriptor (PSD30)	0x00
3071:3040	O	Power State 31 Descriptor (PSD31)	0x00

Table 30. Vendor Specific

Bytes	O/M	Description	Default Value
4095:3072	O	Vendor Specific (VS)	0x00

Table 31. Identify Namespace Data Structure & NVM Command Set Specific

Bytes	O/M	Description	Default Value
7:0	M	Namespace Size (NSZE)	TBD[1]
15:8	M	Namespace Capacity (NCAP)	TBD[1]
23:16	M	Namespace Utilization (NUSE)	TBD[1]
24	M	Namespace Features (NSFEAT)	0x1E
25	M	Number of LBA Formats (NLBAF)	0x04
26	M	Formatted LBA Size (FLBAS)	0x00
27	M	Metadata Capabilities (MC)	0x03
28	M	End-to-end Data Protection Capabilities (DPC)	0x1B
29	M	End-to-end Data Protection Type Settings (DPS)	0x00
30	O	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)	0x01
31	O	Reservation Capabilities (RESCAP)	0xAB
32	O	Format Progress Indicator (FPI)	0x00
33	O	Deallocate Logical Block Features (DLFEAT)	0x19
35:34	O	Namespace Atomic Write Unit Normal (NAWUN)	0x0000
37:36	O	Namespace Atomic Write Unit Power Fail (NAWUPF)	0x0000
39:38	O	Namespace Atomic Compare & Write Unit (NACWU)	0x0000
41:40	O	Namespace Atomic Boundary Size Normal (NABSN)	0x0000
43:42	O	Namespace Atomic Boundary Offset (NABO)	0x0000
45:44	O	Namespace Atomic Boundary Size Power Fail (NABSPF)	0x0000
47:46	O	Namespace Optimal IO Boundary (NOIOB)	0x0000
63:48	O	NVM Capacity (NVMCAP)	TBD[1]
65:64	O	Namespace Preferred Write Granularity (NPWG)	0x0000
67:66	O	Namespace Preferred Write Alignment (NPWA)	0x0000
69:68	O	Namespace Preferred Deallocate Granularity (NPDG)	0x0000
71:70	O	Namespace Preferred Deallocate Alignment (NPDA)	0x0000
73:72	O	Namespace Optimal Write Size (NOWS)	0x0000

Bytes	O/M	Description	Default Value
91:74	-	Reserved	0x00
95:92	O	ANA Group Identifier (ANAGRPID)	0x00000000
98:96	-	Reserved	-
99	O	Namespace Attributes (NSATTR)	0x00
101:100	O	NVM Set Identifier (NVMSETID)	0x0000
103:102	O	Endurance Group Identifier (NEDGID)	0x0000
119:104	O	Namespace Globally Unique Identifier (NGUID)	TBD[2]
127:120	O	IEEE Extended Unique Identifier (EUI64)[2]	TBD[2]
131:128	M	LBA Format 0 Support (LBAF0)	0x02090000
135:132	O	LBA Format 1 Support (LBAF1)	0x00000000
139:136	O	LBA Format 2 Support (LBAF2)	0x00000000
143:140	O	LBA Format 3 Support (LBAF3)	0x00000000
147:144	O	LBA Format 4 Support (LBAF4)	0x00000000
151:148	O	LBA Format 5 Support (LBAF5)	0x00000000
155:152	O	LBA Format 6 Support (LBAF6)	0x00000000
159:156	O	LBA Format 7 Support (LBAF7)	0x00000000
163:160	O	LBA Format 8 Support (LBAF8)	0x00000000
167:164	O	LBA Format 9 Support (LBAF9)	0x00000000
171:168	O	LBA Format 10 Support (LBAF10)	0x00000000
175:172	O	LBA Format 11 Support (LBAF11)	0x00000000
179:176	O	LBA Format 12 Support (LBAF12)	0x00000000
183:180	O	LBA Format 13 Support (LBAF13)	0x00000000
187:184	O	LBA Format 14 Support (LBAF14)	0x00000000
191:188	O	LBA Format 15 Support (LBAF15)	0x00000000
383:192	-	Reserved	0x00
4095:384	O	Vendor Specific (VS)	0x00

[1]According to IDEMA SPEC

[2]According to IEEE EUI-64 SPEC

7.3. S.M.A.R.T. ATTRIBUTES

Table 32. S.M.A.R.T. Attributes (Log Identifier 02h)

Bytes Index	Bytes	Description
[0]	1	Critical Warning
[2:1]	2	Composite Temperature
[3]	1	Available Spare
[4]	1	Available Spare Threshold
[5]	1	Percentage Used
[31:6]	26	Reserved
[47:32]	16	Data Units Read
[63:48]	16	Data Units Written
[79:64]	16	Host Read Commands
[95:80]	16	Host Write Commands
[111:96]	16	Controller Busy Time
[127:112]	16	Power Cycles
[143:128]	16	Power On Hours
[159:144]	16	Unsafe Shutdowns
[175:160]	16	Media and Data Integrity Errors
[191:176]	16	Number of Error Information Log Entries
[195:192]	4	Warning Composite Temperature Time
[199:196]	4	Critical Composite Temperature Time
[201:200]	2	Temperature Sensor 1 (Current Temperature)
[203:202]	2	Temperature Sensor 2 (N/A)
[205:204]	2	Temperature Sensor 3 (N/A)
[207:206]	2	Temperature Sensor 4 (N/A)
[209:208]	2	Temperature Sensor 5 (N/A)
[211:210]	2	Temperature Sensor 6 (N/A)
[213:212]	2	Temperature Sensor 7 (N/A)
[215:214]	2	Temperature Sensor 8 (N/A)
[219:216]	4	Thermal Management Temperature 1 Transition Count
[223:220]	4	Thermal Management Temperature 2 Transition Count
[227:224]	4	Total Time for Thermal Management Temperature 1 (seconds)
[231:228]	4	Total Time for Thermal Management Temperature 2 (seconds)
[511:216]	280	Reserved

Table 33. S.M.A.R.T. Attributes (Log Identifier C0h)

Bytes Index	Bytes	Description
[7:0]	8	Device Capacity
[15:8]	8	User Capacity
[23:16]	8	NAND Read
[31:24]	8	NAND Write
[39:32]	8	NAND Erase Sector
[47:40]	8	Wear Range Delta (%)
[55:48]	8	SSD Life Used Percent D3
[56]	1	WP Water Mark
[58:57]	2	Highest Temperature
[64:59]	8	Flash UNC Error Count
[68:65]	4	Data E3D Error
[72:69]	4	PHY Error Count
[76:73]	4	Total Bad Block Count
[80:77]	4	Total Early Bad Block Count
[84:81]	4	Total Later Bad Block Count
[88:85]	4	Read Fail Count
[92:89]	4	Program Fail Count
[96:93]	4	Erase Failure Count
[104:97]	8	System Table Copy Count
[112:105]	8	ReadMoveTableCnt
[116:113]	4	Data Read Retry Count
[120:117]	4	RAID ECC Retry Count
[124:121]	4	RAID ECC Failed Count
[132:125]	8	Total Erase Count
[136:133]	4	D2/D3 Max Erase Count
[140:137]	4	D2/D3 Average Erase Count
[144:141]	4	D2/D3 Min Erase Count
[152:145]	8	Background Read Count
[156:153]	4	Host Write Uncorrectable Sector Count
[160:157]	4	PS3 Enter Success
[164:161]	4	PS4 Enter Success
[168:165]	4	Wear Leveling Count
[170:169]	2	Chip Internal Temperature
[172:171]	2	Thermal Throttling
[174:173]	2	Thermal Throttling Time
[176:175]	8	FW Code Update Count

Bytes Index	Bytes	Description
[177]	1	Current D1 SSD Live Used Percent
[511:178]	326	Reserved

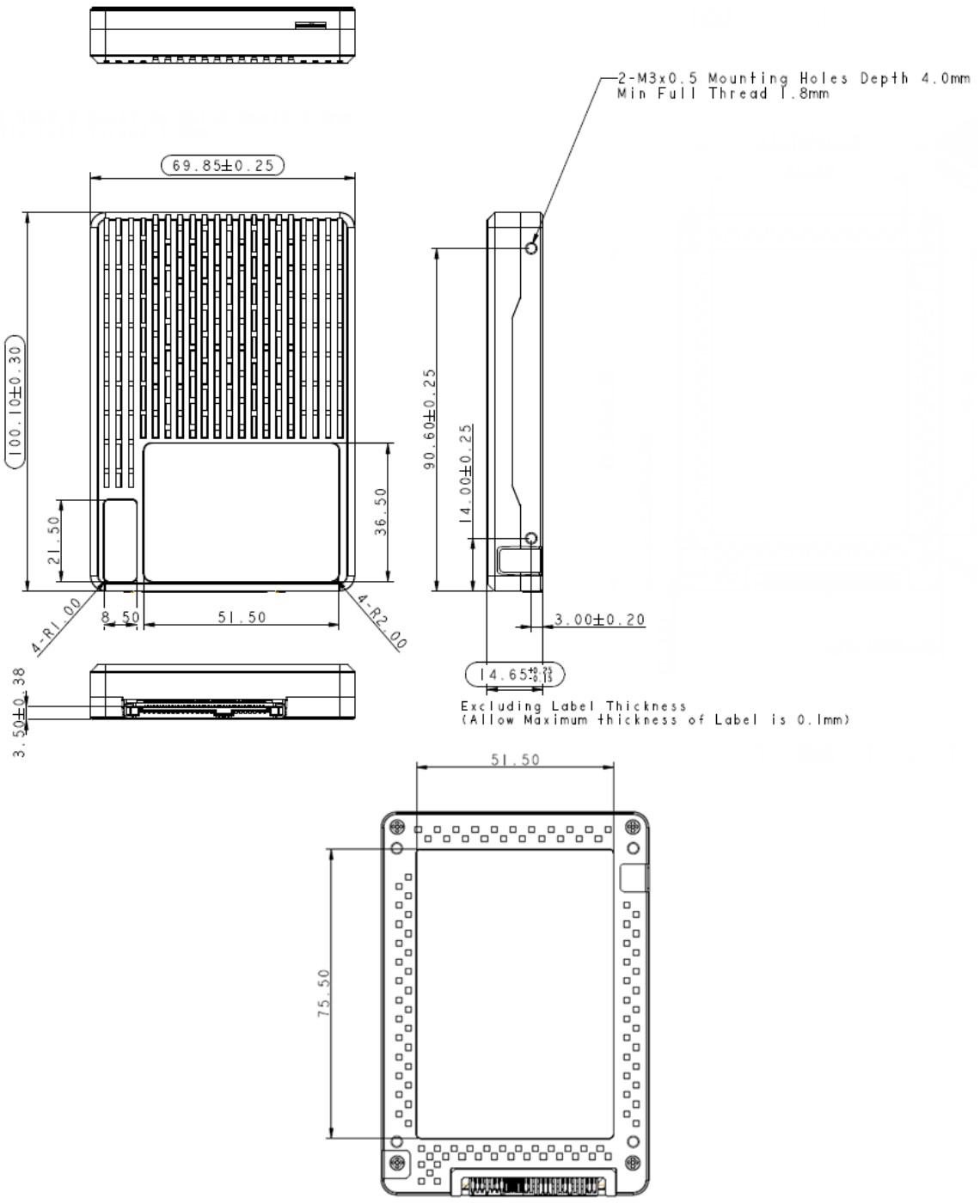
Table 34. S.M.A.R.T. Attributes (Log Identifier D2h)

Bytes Index	Bytes	Description
[7:0]	8	Device Capacity
[15:8]	8	User Capacity
[23:16]	8	NAND Read
[31:24]	8	NAND Write
[39:32]	8	NAND Erase Sector
[47:40]	8	Wear Range Delta (%)
[55:48]	8	SSD Life Used Percent D3
[56]	1	WP Water Mark
[58:57]	2	Highest Temperature
[62:59]	4	Read Fail Count
[66:63]	4	Data E3D Error
[70:67]	4	PHY Error Count
[74:71]	4	Total Bad Block Count
[78:75]	4	Total Early Bad Block Count
[82:79]	4	Total Later Bad Block Count
[86:83]	4	Read Fail Count
[90:87]	4	Program Fail Count
[94:91]	4	Erase Failure Count
[102:95]	8	System Table Copy Count
[110:96]	8	ReadMoveTableCnt
[114:111]	4	Data Read Retry Count
[118:115]	4	RAID ECC Retry Count
[122:119]	4	RAID ECC Failed Count
[130:123]	8	Total Erase Count
[134:131]	4	D2/D3 Max Erase Count
[138:135]	4	D2/D3 Average Erase Count
[142:139]	4	D2/D3 Min Erase Count
[150:143]	8	Background Read Count (N/A)
[154:151]	4	Host Write Uncorrectable Sector Count
[158:155]	4	PS3 Enter Success (N/A)
[162:159]	4	PS4 Enter Success (N/A)
[166:163]	4	Wear Leveling Count
[168:167]	2	Chip Internal Temperature
[170:169]	2	Thermal Throttling
[172:171]	2	Thermal Throttling Time
[180:173]	8	FW Code Update Count

Bytes Index	Bytes	Description
[188:181]	8	Flash UNC Error Count
[192:189]	4	HB Retry Count
[196:193]	4	SB Retry Count
[511:197]	315	Reserved

8. PHYSICAL DIMENSION

Figure 7. U.2 / U.3 2.5-inch 15mm Mechanical Information

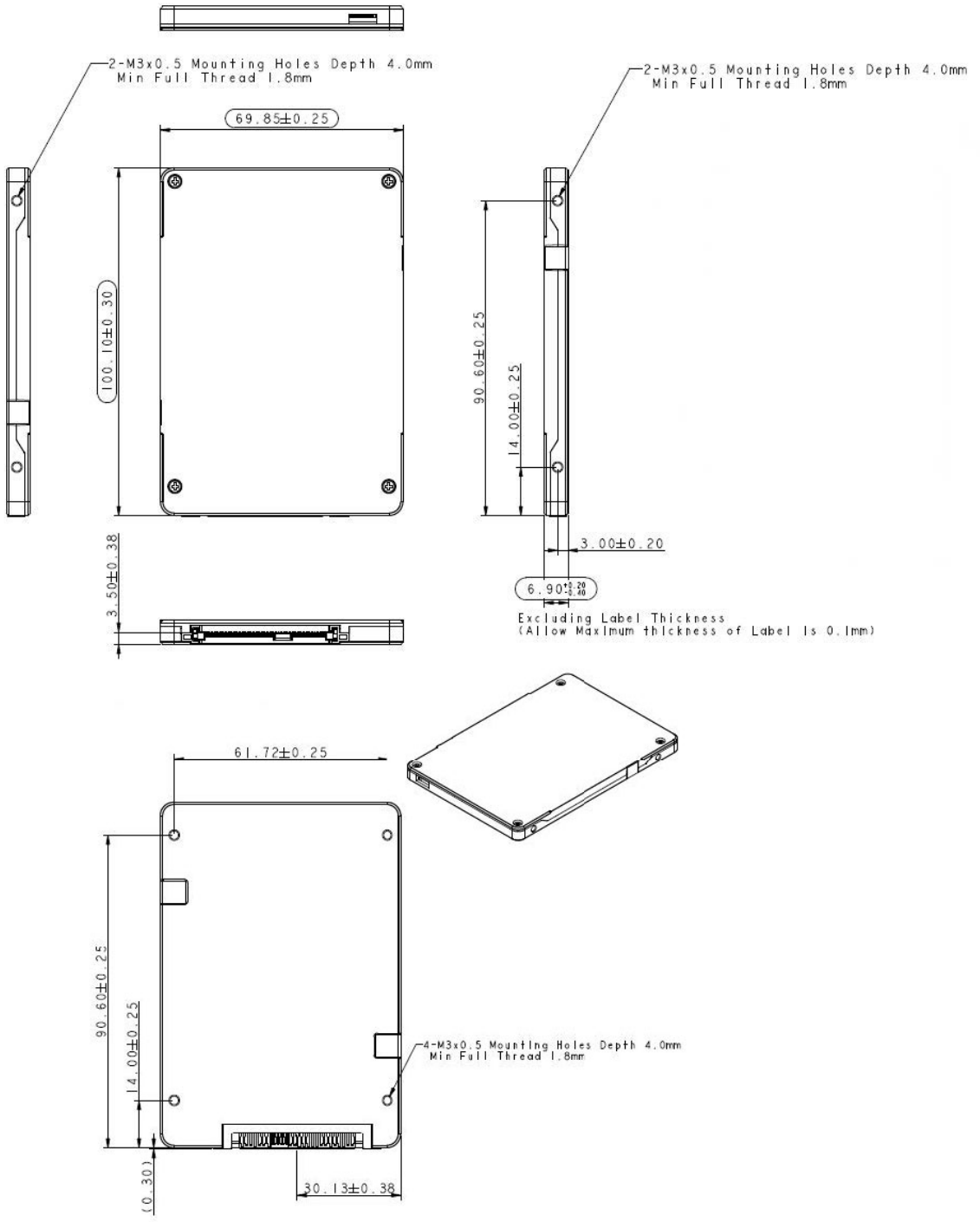


This figure shows the case mechanical information of a U.2 / U.3 2.5-inch 15mm SSD. All dimensions are in millimeters.

Table 35. U.2 / U.3 2.5-inch 15mm Length/Width/Height

	Nominal (mm)	Tolerance (mm)
Length	100.1	± 0.30
Width	69.85	± 0.25
Height	14.65	± 0.25 / -0.15

Figure 8. U.2 / U.3 2.5-inch 7mm Mechanical Information



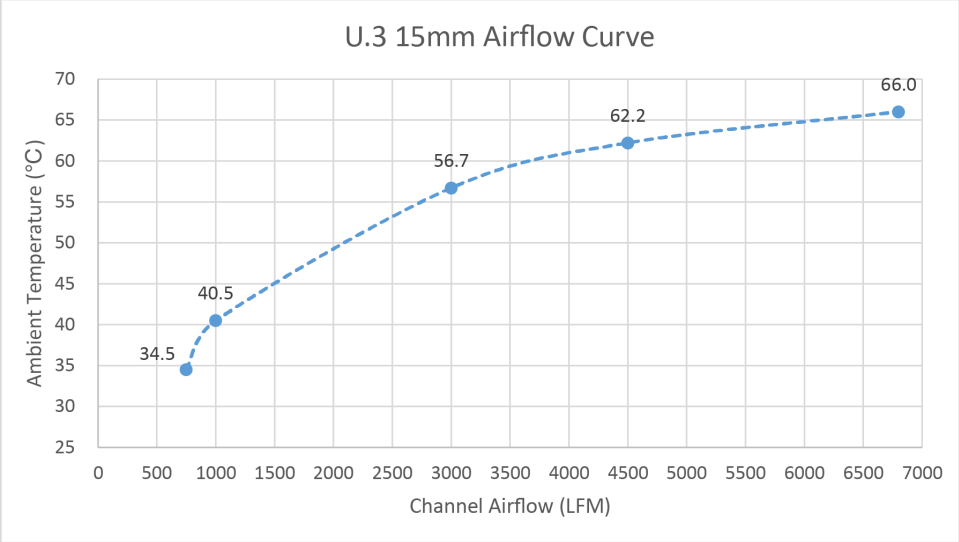
This figure shows the case mechanical information of a U.2 / U.3 2.5-inch 7mm SSD. All dimensions are in millimeters.

Table 36. U.2 / U.3 2.5-inch 7mm Length/Width/Height

	Nominal (mm)	Tolerance (mm)
Length	100.1	± 0.30
Width	69.85	± 0.25
Height	6.9	± 0.20 / -0.40

9. AIR FLOW PROFILE

Figure 9. U.3 15mm Airflow Curve



This figure depicts the minimum airflow a U.3 15mm (8TB) needs to operate without triggering thermal throttling at ambient temperatures varied from 35°C to 65°C.

10. PERFORMANCE AND POWER SOP

The methodologies and platform used to obtain the power and performance numbers will be listed in the following sections. Again, performance and power may differ according to the flash configuration and platform used.

10.1. PERFORMANCE TEST PLATFORM

- Motherboard: X570 AORUS MASTER Default string
- CPU: AMD Ryzen 7 5800X 8-Core Processor
- DRAM: DDR4 3200MHz 16GB
- OS Version: Windows 10 (10.0) Professional 64-bit

10.2. PERFORMANCE METHODOLOGIES

10.2.1. FIO TEST PROCEDURE

Secure erase → no need format drive - 128K Seq. write/read

1. Pre-con - 300% seq. write to full disk
   a. IO Depth = 32
   b. Number of jobs = 1
2. Test script
   a. IO Depth = 32
   b. Number of Jobs= 1
   c. Test duration: 300secs

10.2.2. IOPS CONSISTENCY TEST PROCEDURE

Secure erase → no need format drive - 4K random write/read

1. Pre-con - 300% 4K random. write to full disk
   a. IO Depth = 1
   b. Number of jobs = 1
2. Pre-con - 300% 4K random. write to full disk
   a. IO Depth = 32
   b. Number of Jobs= 1
3. Pre-con - 300% 4K random. write to full disk
   a. IO Depth = 64
   b. Number of Jobs= 8

10.2.3. LATENCY TEST PROCEDURE

Secure erase → no need format drive - 4K random write/read

1. Pre-con - 300% 4K random. write to full disk
   a. IO Depth = 1
   b. Number of jobs = 1

2. Pre-con - 300% 4K random. write to full disk
   a. IO Depth = 32
   b. Number of Jobs= 1
3. Pre-con - 300% 4K random. write to full disk
   a. IO Depth = 64
   b. Number of Jobs= 8

10.2.4. QOS TEST PROCEDURE

Secure erase → no need format drive - 4K random write/read

1. Pre-con - 300% 4K random. write to full disk
   a. IO Depth = 1
   b. Number of jobs = 1
2. Pre-con - 300% 4K random. write to full disk
   a. IO Depth = 32
   b. Number of Jobs= 1
3. Pre-con - 300% 4K random. write to full disk
   a. IO Depth = 64
   b. Number of Jobs= 8

Data Collection Procedure

1. Run entire test script one time.
2. Run every condition in this script for 300 seconds.
3. Calculate average value for every condition.
4. Get the average value, add some buffer and round down to the closest 10th.
5. Verify number with what was requested in PRD.

10.3. POWER CONSUMPTION TEST PLATFORM

- Mother board: X570 AORUS MASTER Default string
- CPU: AMD Ryzen 7 5800X 8-Core Processor
- DRAM: DDR4 3200MHz 16GB
- OS Version: Ubuntu 16.04.3 LTS

10.4. POWER CONSUMPTION METHODOLOGIES

10.4.1. TEST PROCEDURE

1T/2T/4T/8T device

- **Secure erase → no need format drive → Connect power board (Measure Current)**
  - 2048k Seq. write/read
    1. Pre-con - 300% seq. write to full disk
       a. IO Depth = 1024
       b. Number of jobs = 1
    2. Test script (100% seq. write / 100% seq. read)
       a. IO Depth = 1024
       b. Number of Jobs= 1

c. Test duration: 900secs (for each performance)

- 4k random write/read
  1. Test script - 100% ran. write / 100% ran. read / 70% ran. read + 30% ran write / 30% ran. read + 70% ran write
     a. IO Depth = 256
     b. Number of Jobs= 12
     c. Test duration: 900secs (for each performance)

16T device

- **Secure erase → no need format drive → Connect power board (Measure Current)**
  - 128k Seq. write/read
    1. Pre-con - 300% seq. write to full disk
       a. IO Depth = 32
       b. Number of jobs = 1
    2. Test script (100% seq. write / 100% seq. read)
       a. IO Depth = 32
       b. Number of Jobs= 1
       c. Test duration: 900secs (for each performance)

  - 4k random write/read
    1. Test script - 100% ran. write / 100% ran. read / 70% ran. read + 30% ran write / 30% ran. read + 70% ran write
       a. IO Depth = 32
       b. Number of Jobs= 8
       c. Test duration: 900secs (for each performance)

- **Data collection procedure - Max Average (10ms resolution)**
  1. Run entire test script one time.
  2. Run every condition in this script.
  3. Calculate average value for every condition then choose maximum average.
  4. Note value for every condition.
  5. 6pcs sample for every capacity.

- **Data collection procedure - Peak (1us resolution)**
  1. Run entire test script one time.
  2. Run every condition in this script.
  3. Choose Maximum Value for every condition
  4. Note the largest value as the Peak.
  5. 6pcs sample for every capacity.

- **Data collection procedure - Power on**
  1. Run power on procedure until drive being ready to use.
  2. Measure power to get Max Ave power and Max Peak power.
  3. 6pcs sample for every capacity.

- **Data collection procedure - Idle**
  1. After completing every condition, Idle for 30 secs.
  2. Measure power to get Max Ave power and Max Peak power.
  3. 6pcs sample for every capacity.

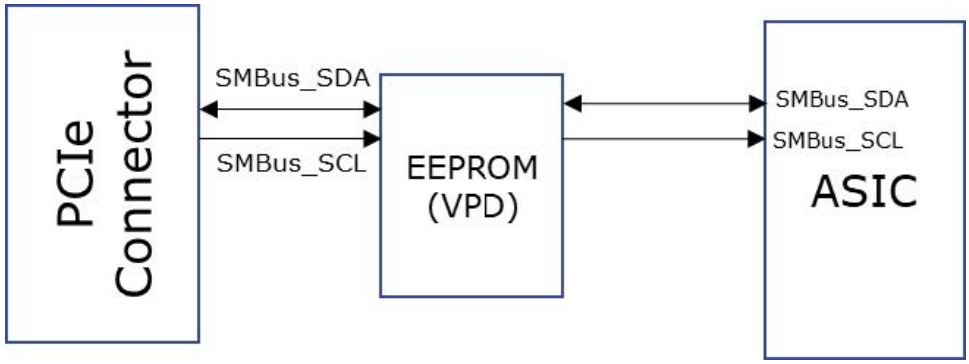
11. VITAL PRODUCT DATA

The TEMPLAR U.3 Enterprise SSD Series can support Read and Write to Vital Product Data (VPD). Please refer to the figure below for details on VPD Data Structure. VPD contains:

- Basic inventory information such as type and size of Enterprise PCIe SSD, manufacture, date, revision, and GUID.
- Power management data such as power level and power modes.
- Vendor specific data.

VPD is stored in a SMBus device with a slave address of 0xA6. VPD page can be read via SMBUS through address 0x53. Writes to the VPD page uses 0x53.

Figure 10. U.3 PCIe SSD Controller Block Diagram



APPENDIX A. PCIE ID

Table A.1. PCIe ID

ID Name	Description	U.3 15mm	PCIe Register Location	Identify Controller Location	Vital Product Data Location
Vendor ID (VID)	Vendor ID assigned by PCI-SIG	0x1BB2	PCI Header Offset 0x2	Identify Controller Data Structure Bytes 01:00	TBD
Device ID (DID)	Device ID assigned by vendor	0x5021	PCI Header Offset 0x0	N/A	TBD
Subsystem Vendor ID	Indicates subsystem vendor ID	0x1986	PCI Header Offset 0x2C	Identify Controller Data Structure Bytes 03:02	TBD
Subsystem ID	Subsystem identifier	0x1986	PCI Header Offset 0x2E	N/A	TBD