FAIRCHILD SEMICONDUCTOR

Good Things Come in Fairchild's FLMP Packages

Fairchild Semiconductor introduces an innovative packaging concept called FlipChip Leaded Molded Package (FLMP).

By James Rana

Fairchild Semiconductor's MOSFETs are now available in FLMP packaging, a concept that achieves a variety of benefits over the standard leaded packages.

Notable Improvements

The package maintains the identical industry footprint and pin-out to several prominent industry-standard leaded packages such as the SO-8, SSOT™-6 (TSOP-6), and SC-75-6. It greatly reduces junction-to-board thermal resistance by placing the backside of the die in direct contact with the PCB. Another improvement is that it significantly lowers the drain inductance, source resistance, source inductance, gate resistance, and gate inductance without moving to new packaging form factors.

The FLMP portfolio is comprised of more than 35 products and continues to grow as the FLMP continues to replace higher profile and larger footprint D-PAK and D2-PAK products. The portfolio includes single MOSFETs, dual MOSFETs, and single SyncFET™ MOSFETs. Products are available in both N- and P-Channel polarities as well as single N-Channel devices containing SyncFET silicon.

The single P-Channel products are ideal for a variety of load management applications and portable charging applications, while the single N-Channel MOSFETs are ideal for isolated and non-isolated DC/DC converter applications, battery charging applications, and load management. This unique package is constructed

FLMP MOSFETs Combine Thermal Performance with Ultra-Low Package Resistance.

using the solder-bump technology that Fairchild Semiconductor pioneered with its MOSFET BGAs. In addition, dual P-Channel MOSFETs are ideal for Li-ion battery pack protection circuits.

Conventional Packages vs. FLMP Package

A conventional SO-8 package is constructed using wire-bond technology. Wireless versions of the SO-8 reduce the package resistance and inductance, but don't really improve thermal performance. The FLMP accomplishes both goals simultaneously by eliminating the wire-bonds and allowing the PCB heat sink to be in direct contact with the solderable backside of the MOSFET die. This new package reduces the thermal resistance below 0.5 degrees C/W, a dramatic improvement from the junction-to-lead thermal resistance of 25 degrees C/W found in conventional SO-8 packages. Thermal resistance is also improved by providing heat conduction from both the drain contact on the bottom of the package and the source leads, which are thermally well coupled to the MOSFET source.

The Fairchild Semiconductor FLMP package is offered in the standard three-source SO-8 footprint to provide greatly improved thermal handling capabilities while maintaining compatibility with the SO-8 pin-out assignments. The FLMP SO-8 package is also offered in a unique seven-source pin-out that provides the lowest package inductance and resistance contribution combined with the highest current handling available for any standard outline SO-8 in the industry.

For more information, visit www.arrow.com/resource.

Part Number	Description	Qg	Vds	Rds(on) MAX at Vgs=10V	Rds(on) MAX at Vgs=4.5V	Rds(on) MAX at Vgs=2.5V
FDC3616N	100V N-Channel PowerTrench® MOSFET	23	100 V	0.07	n/a	n/a
FDC6000NZ	Dual N-Channel 2.5V Specified PowerTrench MOSFET	8	20 V	n/a	0.02	0.028
FDC796N	30V N-Channel PowerTrench MOSFET	14	30 V	0.009	0.012	n/a
FDJ128N	N-Channel 2.5Vgs Specified PowerTrench MOSFET	5	20 V	n/a	0.035	0.051
FDJ129P	P-Channel -2.5Vgs Specified PowerTrench MOSFET	4	-20 V	n/a	0.07	0.12
FDS7066SN3	30V N-Channel PowerTrench SyncFET™	41	30 V	0.0055	0.006	n/a